11. The memory device according to Claim 7, wherein the write gate in series with the first sense amplifier is a different write gate from the write gate positioned in series with the second sense amplifier.

12. The memory device according to Claim 7, further comprising a switch positioned between the first sense amplifier and the memory cell, wherein closing the switch allows data to be transferred between the memory cell and the sense amplifier.

13. The memory device according to Claim 12, further comprising a second switch positioned between the second sense amplifier and the memory cell, wherein closing the second switch allows data to be transferred between the memory cell and the second sense amplifier.

REMARKS

Applicant is in receipt of the detailed Office Action mailed October 21, 2002. Claims 1-6 are pending before entry of this amendment. Claims 7-13 have been added. Applicant requests reconsideration of the remaining claims in view of the following remarks.

NEW CLAIMS

New Claims 7-13 have been added. Applicant hereby submits that new claims 7-13 are likewise in a condition for allowance.

35 U.S.C. § 112 Rejection

Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants have amended Claim 1 to further clarify the language rejected by the Examiner. Applicants have amended the claims for clarification purposes only. No modification in claim scope or range of equivalents is intended through these changes. Withdrawal of the rejection is therefore respectfully requested.

35 U.S.C. § 102 Rejection

Claims 1-6 are rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Publication No. 2002-0003263 to Tanizaki. The Examiner refers to the prior art section of Tanizaki, specifically Figures 13 and 14, to state that the cited reference includes all of the elements recited in the claims. Applicant respectfully traverses the rejection.

Figure 13 of Tanizaki generally shows a matrix of memory cells for a DRAM device. Figure 14 illustrates bit lines connecting memory devices to write drivers 37 and read amplifiers 38 through one sense amplifier 47 and two switching devices 50 and 60. However, Tanizaki fails to disclose the memory devices being connected to the read amp or write driver through *at least two parallel sense amplifiers* as claimed in the present application. Instead, Tanizaki teaches only one sense amplifier 47 connecting bit lines from a memory cell. Although Tanaziaki uses two switches 50 and 60, it does not teach using two sense amplifiers. In fact, Tanazaki is more akin to Figure 1 described in the background section of the present application than for the claimed invention.

The claimed invention, contrarily, claims sense amplifiers positioned in parallel to provide parallel connections between the memory cell and respective read or write data bus. Claim 1 recites this feature as "a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells..." As described on page 7 of the present application, this is what allows data to be read out successively when the activated word line is switched to a new word line. This matrix of parallel sense amplifiers allows reduced architecture real-estate while reducing access time. New Claims 8-13 similarly recite this feature and are likewise in condition for allowance. Accordingly, for the reasons set forth above, Applicant submits that claims 1-7 and new claims 8-13 are in a condition for allowance.

CONCLUSION

For at least the above reasons, Applicants respectfully submits that the present invention, as claimed, is patentable over the prior art. If the Examiner has any issues which he believes can be expedited by a telephone conference, he is encouraged to telephone the undersigned Representative.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance, and a Notice to that effect is earnestly solicited.

It is believed that any additional fees due with respect to the filing of this paper should be identified in any accompanying transmittal. However, if any additional fees are required in connection with the filing of this paper that are not identified in any accompanying transmittal, permission is given to charge Deposit Account 18-0013 in the name of Rader, Fishman & Grauer PLLC.

Respectfully submitted,

Dated: January 14, 2003 By:_____

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MARKED-UP CLAIMS

1. (Amended) A memory device comprising:

a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines;

a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines[,] through the pairs of bit lines; and

a read gate and a write gate which are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines,

wherein the memory device is controlled so that read data is read out successively when [a word line to be activated,] another of the plurality of word lines is [switched to another word line to be activated] activated.

Please add new claims 7 through 13 as follows:

7. A memory device comprising:

a plurality of memory cells;

a plurality of sense amplifiers;

a plurality of read gates communicating with a read bus;

a plurality of write gates communicating with a write bus;

wherein each of the memory cells connects to the read bus through a read gate and a first sense amplifier that are positioned in series;

wherein each of the memory cells connects to the read bus through a read gate and a second sense amplifier that are positioned in series;

wherein each of the memory cells connects to the write bus through a write gate and the first sense amplifier that are positioned in series;

wherein each of the memory cells connects to the write bus through a write gate and the second sense amplifier that are positioned in series; and

wherein the first sense amplifier and the second sense amplifier are positioned in parallel, whereby data is able to be transferred through both parallel sense amplifiers during read and write operations.

8. The memory device according to Claim 7, wherein the read gate in series with the first sense amplifier is a same read gate as the read gate positioned in series with the second sense amplifier.

9. The memory device according to Claim 7, wherein the write gate in series with the first sense amplifier is a same write gate as the write gate positioned in series with the second sense amplifier.

10. The memory device according to Claim 7, wherein the read gate in series with the first sense amplifier is a different read gate from the read gate positioned in series with the second sense amplifier.

11. The memory device according to Claim 7, wherein the write gate in series with the first sense amplifier is a different write gate from the write gate positioned in series with the second sense amplifier.

12. The memory device according to Claim 7, further comprising a switch positioned between the first sense amplifier and the memory cell, wherein closing the switch allows data to be transferred between the memory cell and the sense amplifier.

13. The memory device according to Claim 12, further comprising a second switch positioned between the second sense amplifier and the memory cell, wherein closing the second switch allows data to be transferred between the memory cell and the second sense amplifier.